

# AVB Audio IP Platform Overview



## 1. Introduction

The Lab X Technologies AVB Audio IP platform provides a high-channel-capacity audio implementation of IEEE1722, the standards-based next generation of networked audio and video connectivity. AVB provides a number of benefits over existing, proprietary audio networking technologies:

- Open, standards-based protocols
- Supports a heterogeneous network for media, control, and legacy traffic
- Reservation-based bandwidth management ensures QoS for media traffic
- Supports an arbitrary number of media clock domains
- Inherent time-synchronization of endpoints, enabling time-sensitive control applications
- Future extensibility for any isochronous data (audio, video, telemetry, etc.)

In addition to furnishing AVB audio connectivity, the AVB Audio platform also serves as an excellent starting point for highly-integrated digital audio products. At the heart of the platform is an FPGA, which contains a host microprocessor, Lab X AVB Audio IP blocks, audio interface and clock logic, as well as any other peripherals required by the system. FPGA densities and performance have reached the point at which they are capable of implementing entire systems, governing the behavior of an entire product.

The ability to embed AVB network connectivity as well as user interface, audio processing, and other functionality into a single low-cost device opens the door to a wide array of novel products at prices the market will bear.

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## 2. Platform Hardware

While the AVB Audio IP platform covers a breadth of disciplines, it is useful to begin its description with a prototypical hardware system. Figure 1 depicts a board-level block diagram of an AVB audio system:

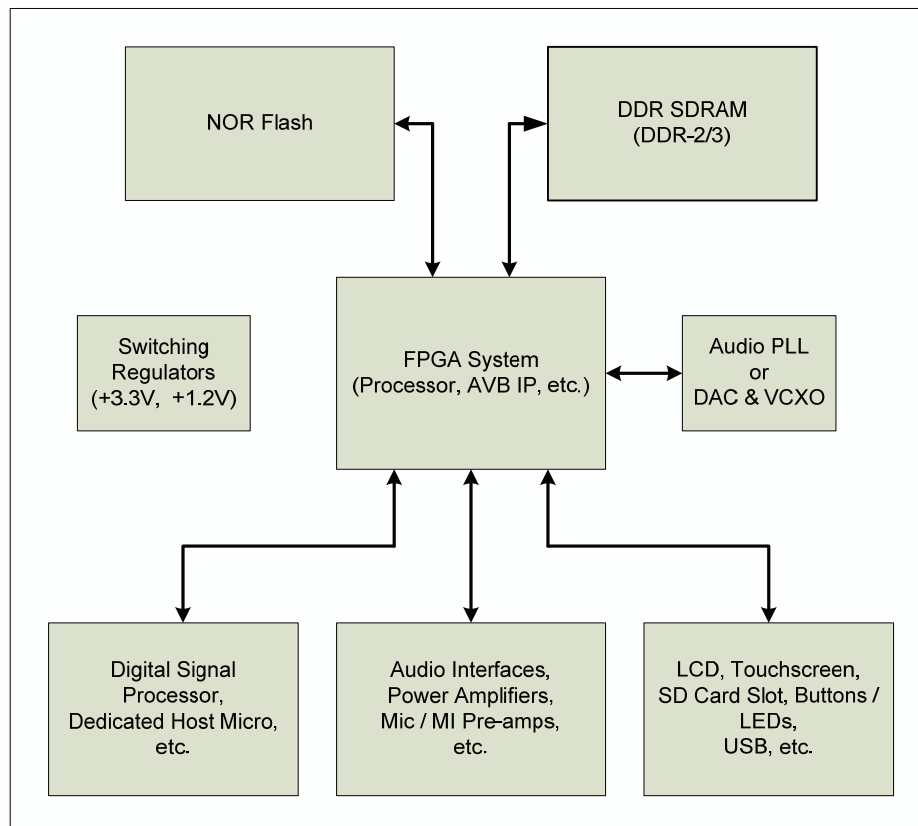


Figure 1- Example AVB Audio System Hardware

At the board level, an Ethernet physical layer device (PHY) is required to attach to the media of choice, typically Category-5 UTP, “Cat5 cable”. Both volatile and non-volatile storage are required to permit the on-chip processor to boot uCLinux. It is important to note that, while Lab X distributes uCLinux device drivers with the AVB Audio solution and employs uCLinux on demonstration boards, use of uCLinux or even an FPGA-embedded processor is *not* necessary. An external host processor or DSP may be used, as long as FPGA gateway is developed to permit the external host to read and write the FPGA-based peripherals, and respond to their interrupt requests. The device drivers will, of course, need to be ported to the chosen supervisory processor. In anticipation of this, all of the device drivers and application interface library code have been written using portable C and C++, respectively.

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AVB permits the presence of an arbitrary number of clock domains on the network, which is a significant departure from other, proprietary networked audio protocols, which enforce the existence of only a single domain. In most cases, each node on the network will need to be capable of being either a master or a slave in each domain. A stable crystal reference is required for master capability, while a phase-lock loop (PLL) is required to recover an audio clock as a slave. A crystal and an integrated PLL may be used, respectively, or a voltage-controlled crystal oscillator (VCXO) with a serial control DAC can be used to play both roles.

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## 3. Platform Gateware

Several Lab X IP gateware modules are instantiated at the FPGA top level, and work together to provide a bi-directional, AVB-compliant audio endpoint. Figure depicts a prototypical Xilinx FPGA design incorporating Lab X AVB Audio platform modules:

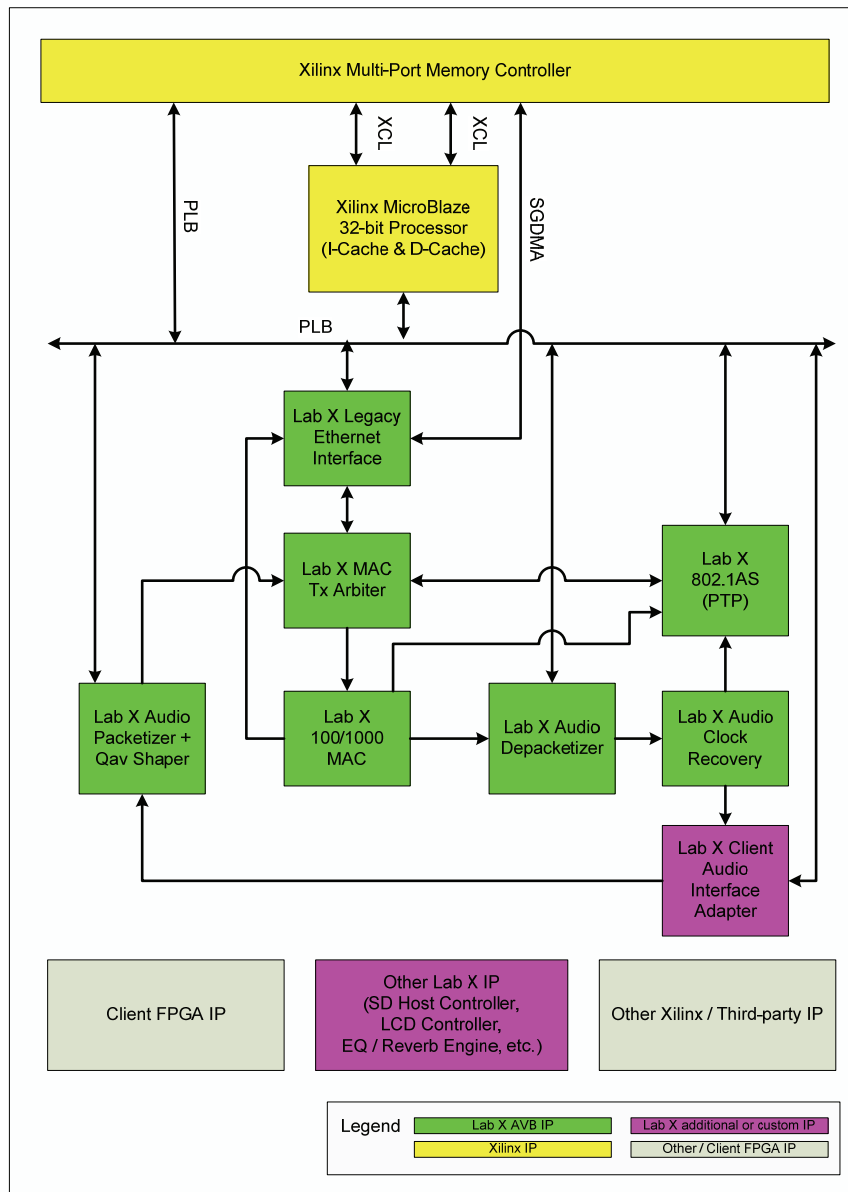


Figure 2 – Example AVB Audio System Gateware

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Each of the gateway modules in Figure performs a role in the implementation of a bi-directional AVB audio endpoint. The supervisory microprocessor's chief roles are: the dynamic configuration of each of the gateway modules in a system-specific manner (i.e. set up and tear down audio streams), and the handling of software protocols. Each of the gateway modules and the relevant software protocols are described in detail in the following subsections of this document.

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## 4. Feature List

Feature	Xilinx EAVB	Lab X AVB Audio IP Platform
802.1 AS Synchronization	X	X
100 MB / 1 GB Operation	X	X
Interface to Xilinx “soft” TMAC	X	X
Interface to Xilinx “hard”	X	X
Interface to Lab X “Simplified soft” MAC		X
RX splitting of raw packets, media vs. legacy packets	X	(handled in Lab X de-packetizer)
Strict priority Tx arbiter for media vs. legacy packets	X	X
802.1Qav credit based output stream shaping	X	X
Multi-stream and class based shaping		X
Multiple domain audio media clock recovery		X
High performance Legacy Ethernet XPS peripheral for MicroBlaze		X
High channel count runtime configurable AVBTP audio packetizer micro-engine		X
High channel count runtime configurable AVBTP audio de-packetizer micro-engine		X
AVBTP presentation time alignment of Rx digital audio outputs		X
Stream Reservation Protocols MSRP / MMRP / MAAP		X
Linux device drivers and MicroBlaze uCLinux reference design		X
Object Oriented C++ Application Programming Interface (API) library		X
High Channel count implementations (> 400 input x 400 output channels on 1 GB)		X